WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device having the step of forming a wiring by a damascene method, comprising the steps of:

forming an etching stopper film and an interlayer insulating film in sequence over a conductive layer;

forming a silicon carbide film, a silicon nitride film, or a silicon oxynitride film as a first hard mask over the interlayer insulating film;

forming a silicon oxide film as a second hard mask over the first hard mask;

forming a silicon carbide film or a silicon nitride film as a third hard mask over the second hard mask;

forming a silicon oxide film as a fourth hard mask over the third hard mask;

forming a pattern over the fourth hard mask;

etching the third hard mask with the fourth hard mask;

etching the second hard mask with the third hard mask;

etching the first hard mask with the third hard mask;

forming an opening which reaches the etching stopper film in the interlayer insulating film by etching the interlayer insulating film with the third hard mask;

etching a portion of the etching stopper film which is exposed from the opening formed in the interlayer dielectric; and

embedding a wiring material in the opening.

2. The method for manufacturing the semiconductor device according to claim 1, wherein a low dielectric constant insulating film is used as the interlayer insulating film.

3. The method for manufacturing the semiconductor device according to claim 1, wherein an inorganic insulating film is used as the interlayer insulating film.

4. The method for manufacturing the semiconductor device according to claim 1, wherein a porous insulating film is used as the interlayer insulating film.

5. The method for manufacturing the semiconductor device according to claim 1, wherein a porous silica film is used as the interlayer insulating film.

6. The method for manufacturing the semiconductor device according to claim 1, wherein the etching stopper film is a silicon carbide film or a silicon nitride film.

7. The method for manufacturing the semiconductor device according to claim 1, wherein a thickness of the third hard mask is more than twice that of the first hard mask.

8. The method for manufacturing the semiconductor device according to claim 1, wherein said step of etching the etching stopper film comprises the step of removing the third hard mask.

9. The method for manufacturing the semiconductor device according to claim 1, wherein said step of etching the second hard mask with the third hard mask comprises the step of removing the fourth hard mask.

10. The method for manufacturing the semiconductor device according to claim 1, wherein said step of forming the pattern over the fourth hard mask comprises the steps of:

forming a first pattern over the fourth hard mask with a first resist mask;

removing the first resist mask;

forming a resin film over an entire surface;

forming a pattern over the resin film with a second resist mask;

forming a second pattern over the fourth hard mask with the resin film as a mask; and

removing the resin film.

11. The method for manufacturing the semiconductor device according to claim 10, wherein the first pattern is a wiring trench pattern and the second pattern is a via hole pattern.

12. The method for manufacturing the semiconductor device according to claim 10 further

comprising, after said step of forming the second pattern over the fourth hard mask, the step of etching the third and second hard masks with the resin film.

13. The method for manufacturing the semiconductor device according to claim 11 further comprising, after said step of forming the second pattern over the fourth hard mask, the step of etching the third and second hard masks with the resin film.

14. The method for manufacturing the semiconductor device according to claim 12, wherein said step of etching the third hard mask with the fourth hard mask comprises the step of etching the first hard mask.

15. The method for manufacturing the semiconductor device according to claim 13, wherein said step of etching the third hard mask with the fourth hard mask comprises the step of etching the first hard mask.

16. The method for manufacturing the semiconductor device according to claim 14, wherein said step of etching the second hard mask with the third hard mask comprises the step of forming a hole which is shallower than the thickness of the interlayer insulating film, in the interlayer insulating film.

17. The method for manufacturing the semiconductor device according to claim 15, wherein said step of etching the second hard mask with the third hard mask comprises the step of forming a hole which is shallower than the thickness of the interlayer insulating film, in the interlayer insulating film.

18. The method for manufacturing the semiconductor device according to claim 10, wherein the opening includes a wiring trench portion formed based over the first pattern and a via hole portion formed over the second pattern.

19. The method for manufacturing the semiconductor device according to claim 11, wherein the opening includes a wiring trench portion formed based over the first pattern and a via hole portion formed over the second pattern.